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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,292	03/12/2004	Kyoung-woo Lee	SAM-0560	8218

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Steven M. Mills
MILLS & ONELLO LLP
Suite 605
Eleven Beacon Street
Boston, MA 02108

EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,292	LEE ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *1-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-23 and 27-29* is/are rejected.

7)☒ Claim(s) *24-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II claims 16 – 29 in the reply filed on November 14, 2005 is acknowledged.

2. Claims 1 – 15 were withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group I claims, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on November 14, 2005.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 16 – 20, 22, 23 and 27 – 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsue, US 6,483,142.

Regarding claim 16, Hsue teaches a dual damascene interconnection structure with a metal – insulator – metal capacitor, the structure comprising:

- a via – level intermetal dielectric 116 and a trench – level intermetal dielectric 138 which are sequentially stacked on a substrate (see Fig. 3C);
- a dual damascene interconnection 148 formed in the via – level intermetal dielectric and the trench – level intermetal dielectric, and
- a metal – insulator – metal capacitor 132 formed between the via – level intermetal dielectric and the trench – level intermetal dielectric to include a lower

electrode126a, a dielecttic layer 128a, and an upper electrode 130a (see Fig. 3C) in descriptions in columns 3 – 5.

Regarding claim 17, Hsue teaches a first lower metal interconnection 104a and a second lower metal interconnection 104b, which are formed between the substrate and the via – level intermetal dielectric (see Fig. 3C), a via 124a which is included in the via – level intermetal dielectric 116 to connect the lower electrode 126a and the first lower metal interconnection 104 a, and an upper metal interconnection 148a formed on and connected to the upper electrode 130a, wherein the dual damascene interconnection 148b is connected to the second lower metal interconnection 104b (see Fig. 3C).

Regarding claim 18, Hsue teaches the first lower metal interconnection 104a and the second lower metal interconnection 104b are damascene interconnections buried in an insulating layer 106 formed on the substrate (see Fig. 3C).

Regarding claim 19, Hsue teaches the via is filled 124a in a hole – type opening (see Fig. 3C). This is a product by process claim.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown,* 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Regarding claim 20, Hsue teaches the via is filled 124a in a line – type opening (see Fig. 3C). This is a product by process claim.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown,* 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Regarding claim 22, Hsue teaches the upper electrode 130a is patterned to have a smaller area than that of each of the lower electrode 126a and the capacitor dielectric layer (see Fig. 3C).

Regarding claim 23, Hsue teaches the via is integrally formed with the lower electrode (see Fig. 3C).

Regarding claim 27, Hsue teaches the dual damascene interconnection is formed of copper in column 5, line 33 – 40.

Regarding claim 28, Hsue teaches the via and the dual damascene interconnection are formed of different materials Cu and W in column 4, lines 23 – 24 and in column 5, line 33 – 40.

Regarding claim 29, Hsue teaches the structure further comprising a first lower metal interconnection 104a and a second lower metal interconnection 104b formed between the substrate and the via - level intermetal dielectric, and an upper metal interconnection 148a formed on and connected to the upper electrode 130a, wherein the lower electrode 126a is directly connected to the first lower metal interconnection 104a, and the dual damascene interconnection 148b is connected to the second metal interconnection 104b (see Fig. 3C).

4. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Hsue, US 6,512,260.

Hsue teaches a dual damascene interconnection structure with a metal – insulator – metal capacitor, the structure comprising:

- a via – level intermetal dielectric 116 and a trench – level intermetal dielectric 138 which are sequentially stacked on a substrate (see Fig. 3C);
- a dual damascene interconnection 148 formed in the via – level intermetal dielectric and the trench – level intermetal dielectric, and
- a metal – insulator – metal capacitor 132 formed between the via – level intermetal dielectric and the trench – level intermetal dielectric to include a lower electrode 126a, a dielectric layer 128a, and an upper electrode 130a (see Fig. 2L) in descriptions in columns 3 – 5.

Hsue also teaches a dual damascene interconnection structure with a metal – insulator – metal capacitor, wherein the lower electrode 126a, the dielectric layer, 128a and the upper electrode 130a are patterned to have the same area with reference to Fig. 2L.

Allowable Subject Matter

5. Claims 24 – 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kai, US 6,746,914 teaches an MIM capacitor having dual damascene interconnection.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar
Asok K. Sarkar
December 29, 2005

Primary Examiner